

BOOTSTRAP MOS FOR HIGH VOLTAGE APPLICATIONS

PRIORITY CLAIM AND CROSS-REFERENCE

[0001] This application is a continuation-in-part of the following commonly-assigned U.S. patent application Ser. No. 14/166,475 filed Jan. 28, 2014 and entitled “Embedded JFETs for High Voltage Applications,” which is a continuation of U.S. patent application Ser. No. 13/481,462, filed May 25, 2012, and entitled “Embedded J915FETs for High Voltage Applications,” which applications are hereby incorporated herein by reference.

BACKGROUND

[0002] A bootstrap Metal-Oxide-Semiconductor (MOS) device may be used to protect bootstrap circuits. Accordingly, it is able to withstand high operation voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIGS. 1A through 4C are top views and cross-sectional views of Junction Field-Effect Transistors (JFETs) in accordance with some exemplary embodiments;

[0005] FIG. 5 illustrates an equivalent circuit diagram of the JFET shown in FIGS. 3A through 4C in accordance with some embodiments;

[0006] FIG. 6A illustrates a top view of a bootstrap Metal-Oxide-Semiconductor (MOS) device in accordance with some embodiments; and

[0007] FIGS. 6B and 6C illustrate cross-sectional views of a bootstrap MOS device in accordance with some embodiments.

DETAILED DESCRIPTION

[0008] The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0009] Further, spatially relative terms, such as “underlying,” “below,” “lower,” “overlying,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in

use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0010] A high voltage Junction Field-Effect Transistor (JFET) and a high voltage bootstrap Metal-Oxide-Semiconductor (MOS) device are provided in accordance with various exemplary embodiments. The variations and the operation of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. In the illustrated embodiments, n-type JFETs and n-type bootstrap MOS devices are provided to explain the concept of the embodiments. It is appreciated that the teaching in the embodiments is readily available for the formation of p-type JFETs and p-type bootstrap MOS devices, with the conductivity types of the respective doped regions inverted.

[0011] FIGS. 1A through 1C are a top view and cross-sectional views of JFET 100 in accordance with some exemplary embodiments. Referring to FIG. 1A, which is a top view, JFET 100 includes drain region 20, gate electrode 24, and source region 26. Gate electrode 24 is disposed between drain region 20 and source region 26. A plurality of contacts 30 are formed over and electrically couple to the respective underlying drain region 20, gate electrode 24, and source region 26. Furthermore, High-Voltage N-Well (HVNW) 38, P-Wells 40 (including 40A and 40B), and P-type Buried Layers (PBLs) 42 are also included in JFET 100.

[0012] FIG. 1B illustrates a cross-sectional view of JFET 100 as shown in FIG. 1A, wherein the cross-sectional view is obtained from the plane crossing line 1B-1B in FIG. 1A. JFET 100 is formed over substrate 34, which may be a p-type substrate, for example, although an n-type substrate may also be used. Buried N-Well (BNW) 36 is formed over substrate 34. In some embodiments, BNW 36 is doped with an n-type impurity to an impurity concentration, for example, between about $10^{14}/\text{cm}^3$ and about $10^{17}/\text{cm}^3$. Over BNW 36, HVNW 38 and PW regions 40 are formed. HVNW 38 and PW regions 40 may be doped with an n-type impurity and a p-type impurity, respectively, to impurity concentrations about $10^{14}/\text{cm}^3$ and about $10^{17}/\text{cm}^3$, for example. PBL 42 is formed under HVNW 38 and over BNW 36, and is of p-type. The impurity concentration of PBL 42 may be between about $10^{15}/\text{cm}^3$ and about $10^{17}/\text{cm}^3$. Drain region 20 and source region 26 are heavily doped (represented by a “+” sign) n-type regions, which may have an n-type impurity concentration greater than about $10^{19}/\text{cm}^3$, or between about $10^{19}/\text{cm}^3$ and about $10^{21}/\text{cm}^3$.

[0013] Insulation region 46 is formed over HVNW 38. In some embodiments, insulation region 46 is a field oxide region formed through the oxidation of silicon. In alternative embodiments, insulation region 46 may be a Shallow Trench Isolation (STI) region. A portion of PBL 42 is under and aligned to insulation region 46. The formation of PBL 42 may be used for Reducing Surface electric Field (RESURF), which electric field may be high due to the high voltage applied on drain region 20.

[0014] PW regions 40 include PW regions 40A and PW 40B, which are spaced apart from each other by portions of HVNW 38, in which source region 26 is formed. As shown in FIG. 1A, PW regions 40A also includes PW regions 40A1, 40A2, and 40A3, with each connected to one of PBLs 42. Accordingly, when a voltage is applied to PW regions 40A,